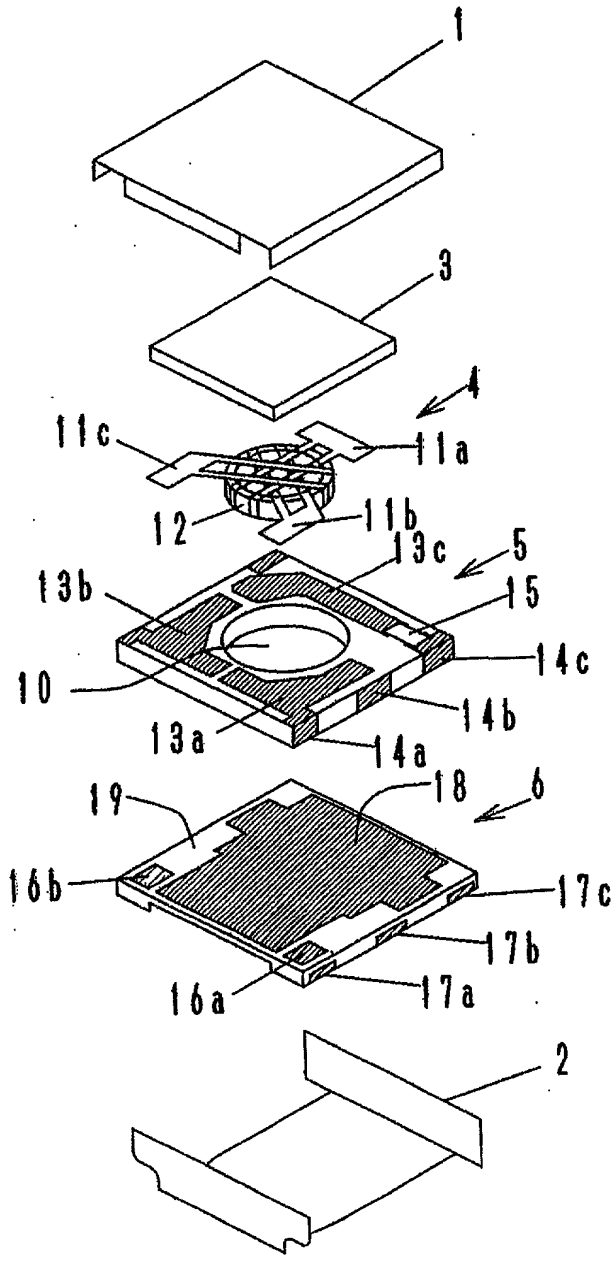


Fig. 1

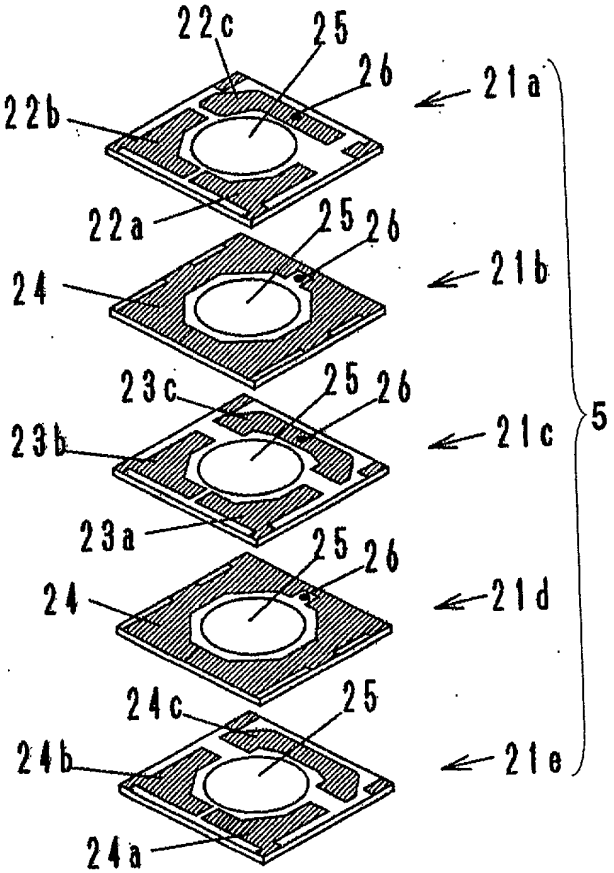


Fig. 2

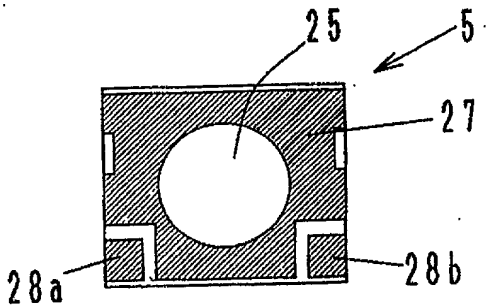


Fig. 3

Fig. 4

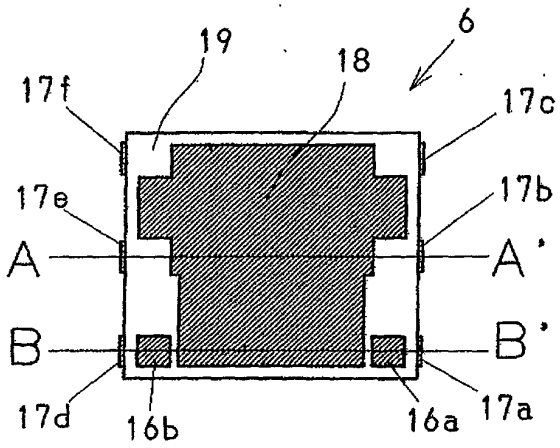


Fig. 5

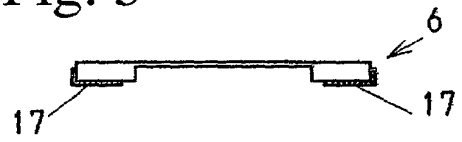


Fig. 6

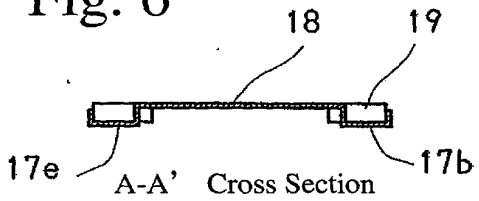


Fig. 7

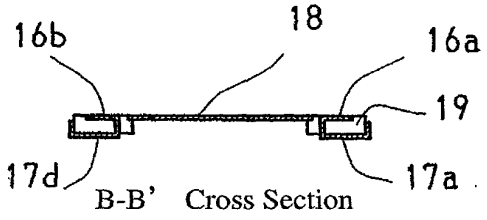


Fig. 8

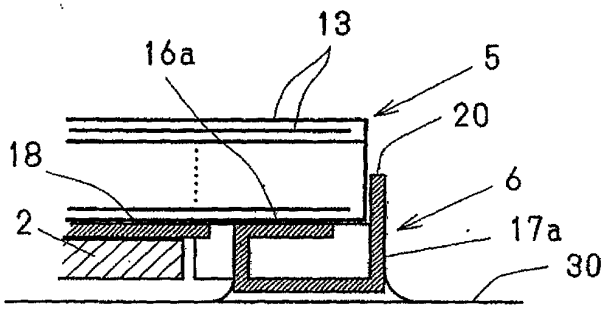


Fig. 11(a)

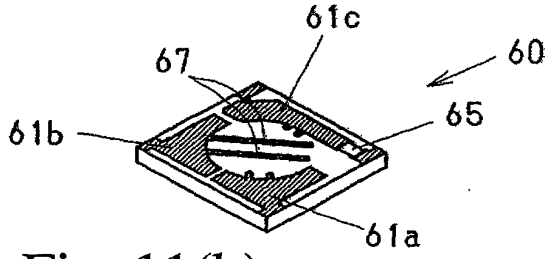
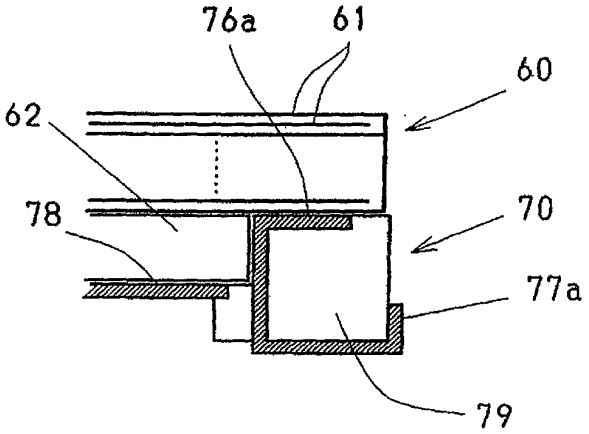


Fig. 11(b)



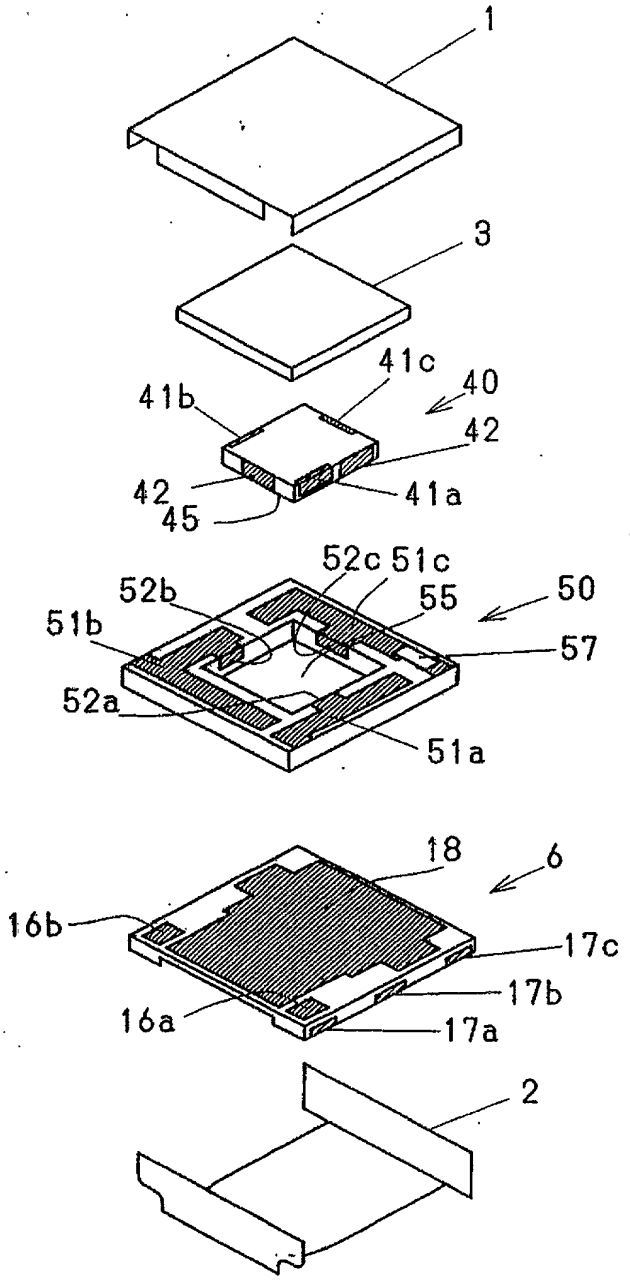

1
3
41c
40
41b
42
42
41a
45
52c
51c
52b
55
50
51b
57
52a
51a
18
6
16b
17c
17b
16a
17a
2

Fig. 9

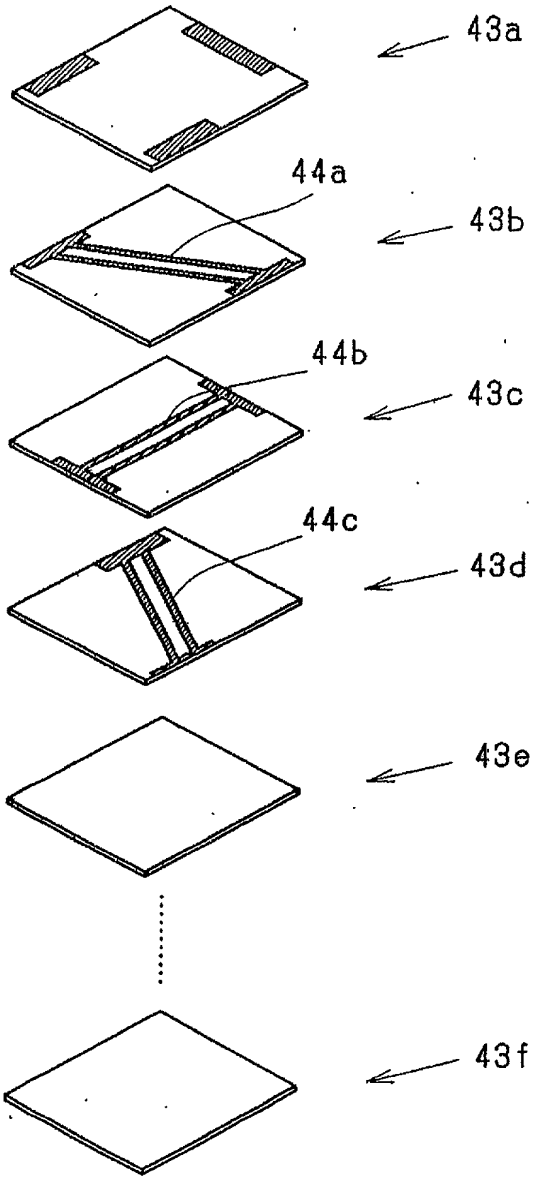

43a
44a
43b
44b
43c
44c
43d
43e
43f

Fig. 10

Fig. 12

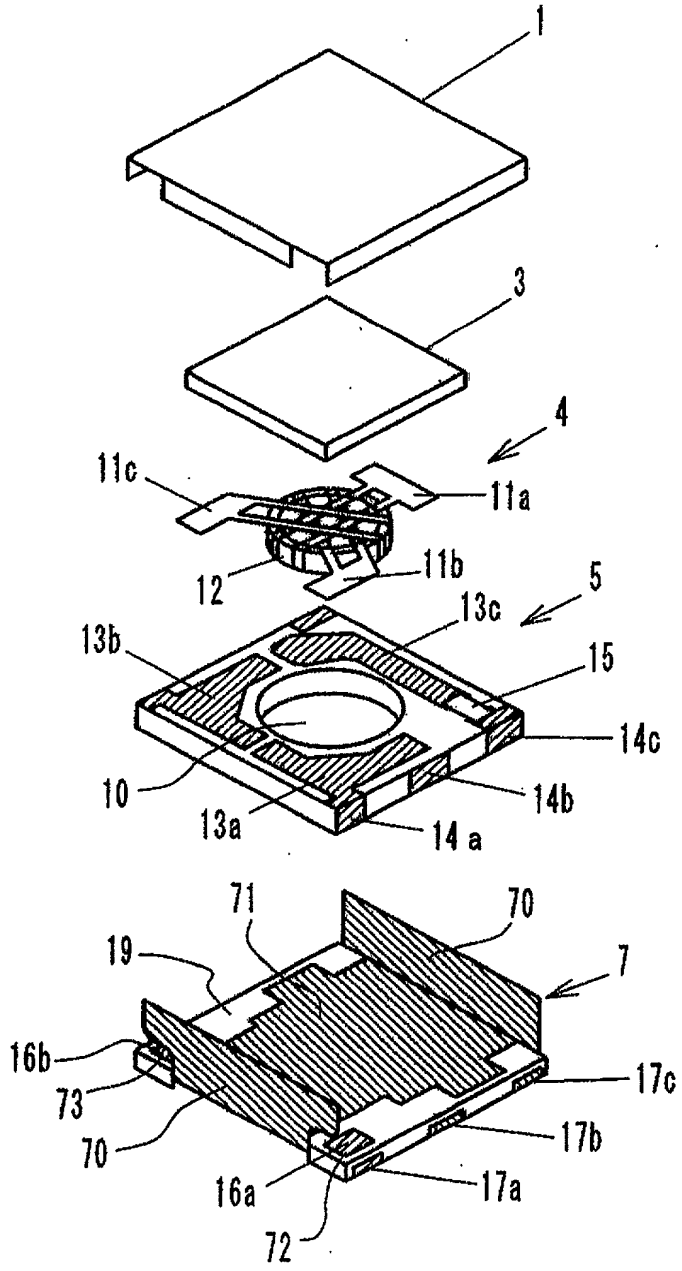
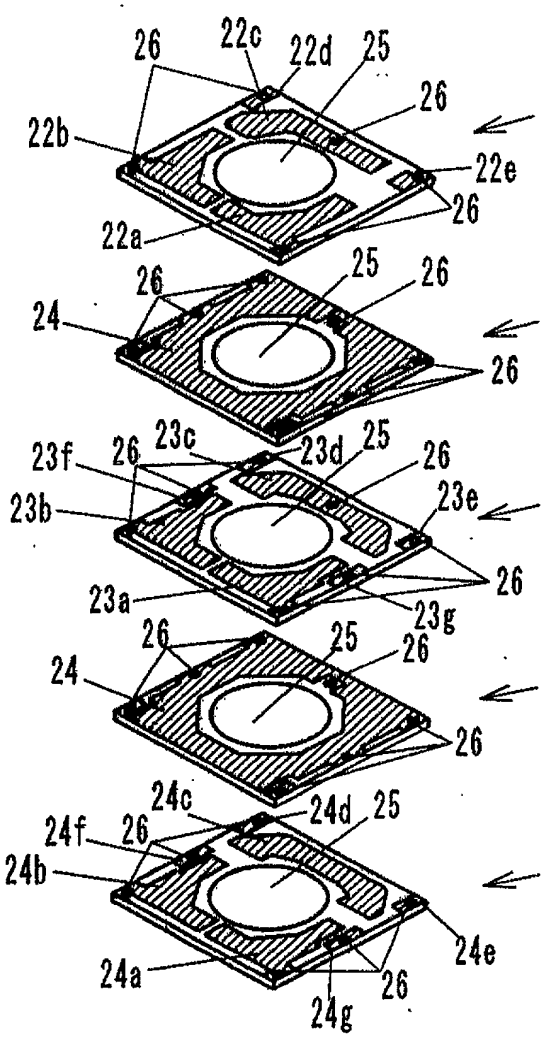

1
3
4
11c
11a
12
11b
5
13c
13b
15
14c
10
14b
13a
14 a
71
70
19
7
16b
17c
73
17b
70
16a
17a
72

Fig. 13


26
22c
22d
25
26
22b
22e
26
22a
26
25
26
24
26
26
23f
26
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23d
25
26
23b
23e
26
23a
23g
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26
24b
24e
24a
26
24g

Fig. 14

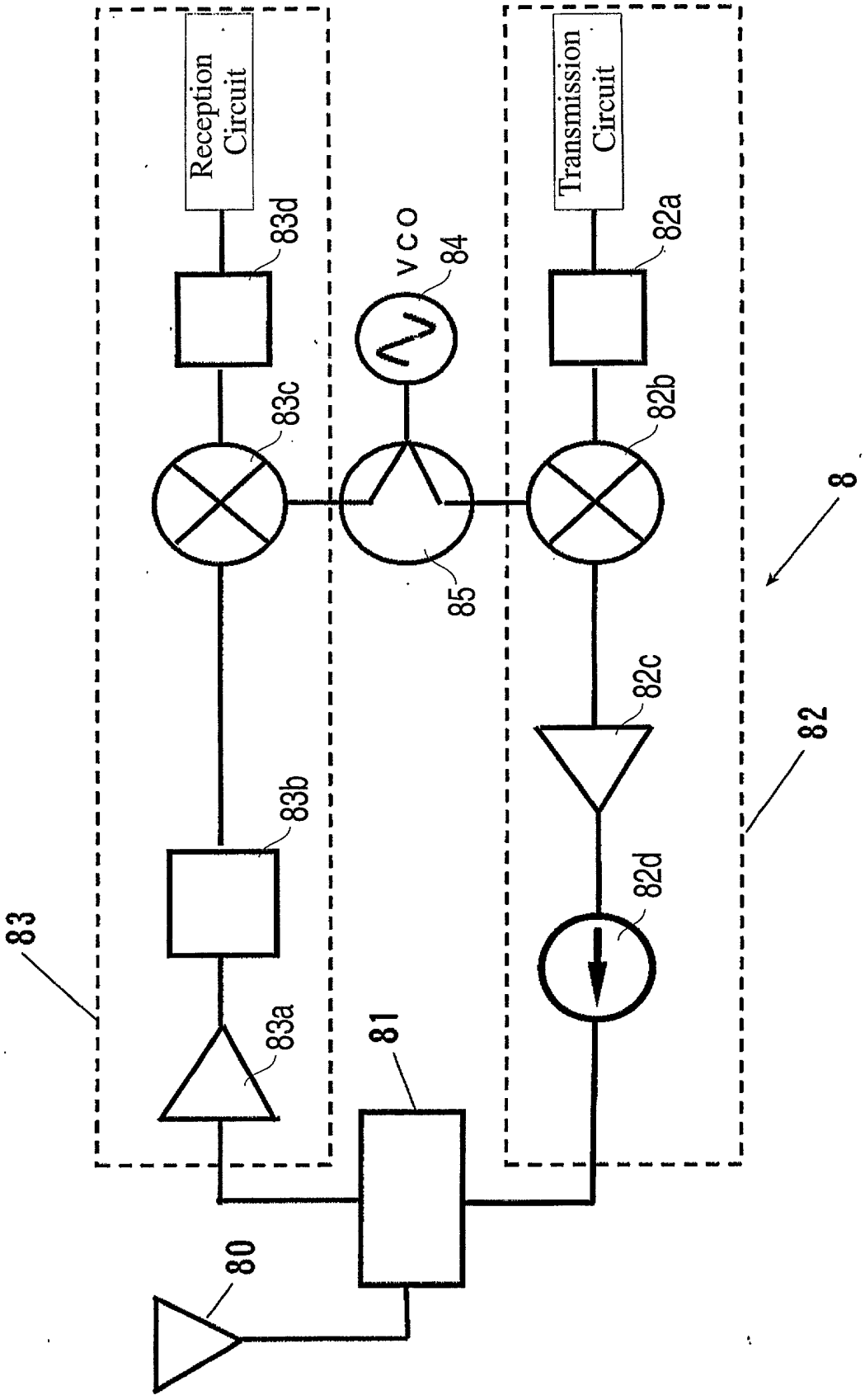
Reception Circuit
Transmission Circuit
VCO
80
81
82
82a
82b
82c
82d
83
83a
83b
83c
83d
84
85
8

Fig. 15

PRIOR ART

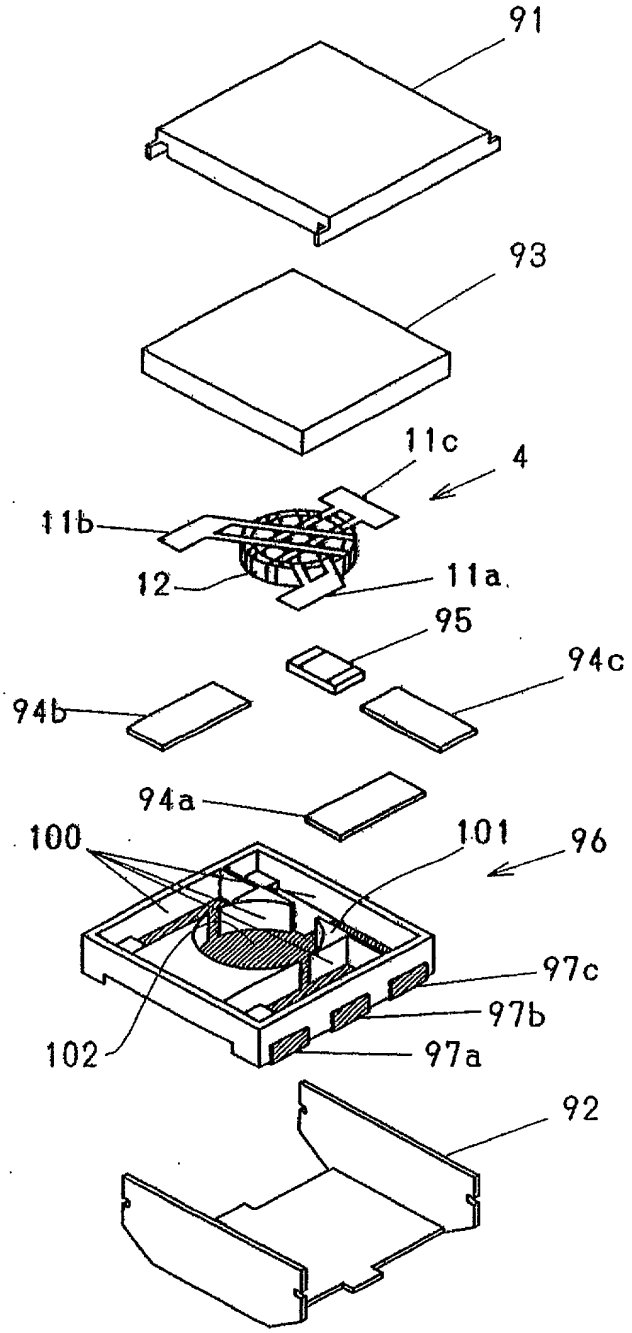

Fig. 16

PRIOR ART